CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of testing a memory device, the method comprising:

selecting a memory cell to be tested from a fringe region of an array of the memory device; and

testing said selected memory cell using at least one test parameter that is different than a test parameter to be used for memory cells not in the fringe region.

2. The method of claim 1, wherein said act of selecting comprises selecting the memory cell from a region that is adjacent to a periphery of said array.

3. The method of claim 1, wherein said act of selecting comprises selecting the memory cell from a region that is adjacent to a folded bitline of said array.

4. The method of claim 1, wherein said at least one parameter is a first voltage level that is different from a voltage level used to test memory cells not in the fringe.

5. The method of claim 4, wherein said first voltage level is different than a supply voltage.

6. The method of claim 5, where said first voltage level is less than approximately 2.5V.

7. The method of claim 1, wherein said act of testing comprises testing said selected memory cell using at least one test parameter more demanding than said test parameter to be used for memory cells not in the fringe region.

8. The method of claim 1, wherein said at least one parameter is a first write recovery time that is different from a second write recovery time used to test memory cells not in the fringe.

9. The method of claim 8, wherein said first write recovery time is shorter than approximately 12 ns.

10. The method of claim 8, wherein said first write recovery time is between approximately 79 – 96% of the second write recovery time.

11. A method of testing a memory device, the method comprising:

selecting a column of a memory array of said memory device to be tested;

selecting a row of said memory array to be tested, said selected column and row defining a memory cell in a fringe region of said memory array;

writing first data to each said memory cell in said memory array;

activating said selected row for reading and writing;

providing second data to a memory cell corresponding to said selected row and selected column, said second data being different from said first data;

precharging said selected row for deactivating said selected row for reading and writing;

activating said selected row for reading and writing;

re-activating said selected row for reading and writing;

providing said first data to said memory cell corresponding to said selected row and selected column, where said first data is provided at a lower voltage than supply voltage, where said first data is provided at a shorter write release time;

reading test data from said memory cell; and

determining if said test data is correct.

12. The method of claim 11, further comprising:

initializing the memory array for access and storage.

13. The method of claim 11, further comprising:

loading a mode register associated with said memory array to establish the write mode.

14. A method of testing an integrated circuit memory, said method comprising:

identifying a first plurality of memory cells of said integrated circuit memory for testing; and

determining if said first plurality of memory cells are weak cells.

15. The method of claim 14, wherein said act of determining comprises stressing said identified first plurality of memory cells to determine if they are weak cells.

16. The method of claim 15, wherein said act of stressing comprises applying a test voltage at a level below a test voltage used for other memory cells of said integrated circuit memory.

17. The method of claim 15, wherein said act of stressing comprises applying a shorter than standard write release time.

18. The method of claim 14, wherein said first plurality of memory cells comprises memory cells located in a row adjacent to a top edge of said memory.

19. The method of claim 14, wherein said first plurality of memory cells comprises memory cells located in a row adjacent to a bottom edge of said memory.

20. The method of claim 14, wherein said first plurality of memory cells comprises memory cells located in a row adjacent to a folded digitline of said memory.

21. The method of claim 14, wherein said first plurality of memory cells comprises memory cells located in a column adjacent to at least one of a right edge and a left edge of said memory.

22. The method of claim 14, wherein said first plurality of memory cells comprises memory cells located in at least one of a first and second row of memory adjacent to an edge of said memory.

23. The method of claim 22, wherein said second row of memory is adjacent to said first row of memory.

24. The method of claim 22, wherein said second row of memory is not adjacent to said first row of memory.

25. The method of claim 22, wherein said edge of said memory is a top edge of said memory.

26. The method of claim 22, wherein said edge of said memory is a bottom edge of said memory.

27. The method of claim 14, wherein said first plurality of memory cells comprises memory cells located in at least one of a first and second column of memory adjacent to an edge of said memory.

28. The method of claim 27, wherein said second column of memory is adjacent to said first column of memory.

29. The method of claim 27, wherein said second column of memory is not adjacent to said first column of memory.

30. The method of claim 27, wherein said edge of said memory is a right edge of said memory.

31. The method of claim 27, wherein said edge of said memory is a left edge of said memory.

32. A system for testing memory devices, comprising;

test control circuitry; and

connecting circuitry that connects the test control circuitry to a memory device under test;

the test control circuitry providing signals through the connecting circuitry to:

select a memory cell to be tested from a fringe region of an array of the memory device; and

test said selected memory cell using at least one test parameter that is different than a test parameter to be used for memory cells not in the fringe region.

33. A system for testing memory devices, comprising;

test control circuitry; and

connecting circuitry that connects the test control circuitry to a memory device under test;

the test control circuitry providing signals through the connecting circuitry to:

select a column of a memory array of said memory device to be tested;

select a row of said memory array to be tested, said selected column and row defining a memory cell in a fringe region of said memory array;

write first data to each said memory cell in said memory array;

activate said selected row for reading and writing;

provide second data to a memory cell corresponding to said selected row and selected column, said second data being different from said first data;

precharge said selected row for deactivating said selected row for reading and writing;

activate said selected row for reading and writing;

re-activate said selected row for reading and writing;

provide said first data to said memory cell corresponding to said selected row and selected column, where said first data is provided at a lower voltage than supply voltage, where said first data is provided at a shorter write release time;

read test data from said memory cell; and

determine if said test data is correct.

34. A system for testing memory devices, comprising;

test control circuitry; and

connecting circuitry that connects the test control circuitry to a memory device under test;

the test control circuitry providing signals through the connecting circuitry to:

identify a first plurality of memory cells of said integrated circuit memory for testing; and

determine if said first plurality of memory cells are weak cells.